MARACAS: A Real-Time Multicore VCPU Scheduling Framework

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Overview

Introduction

Quest RTOS

Background Scheduling

Memory-Aware Scheduling

Multicore VCPU Scheduling

Evaluation

Conclusion

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2. Quest RTOS
3. Background Scheduling
4. Memory-Aware Scheduling
5. Multicore VCPU Scheduling
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- Multicore platforms are gaining popularity in embedded and real-time systems
  - concurrent workload support
  - less circuit area
  - lower power consumption
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- Complex on-chip memory hierarchies pose significant challenges for applications with real-time requirements

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- Shared cache contention:
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  - bank-aware memory management
  - memory throttling

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- We proposed a new bus monitoring metric that accurately detects traffic

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- Mixed-criticality systems running performance-demanding applications
  - machine learning
  - computer vision

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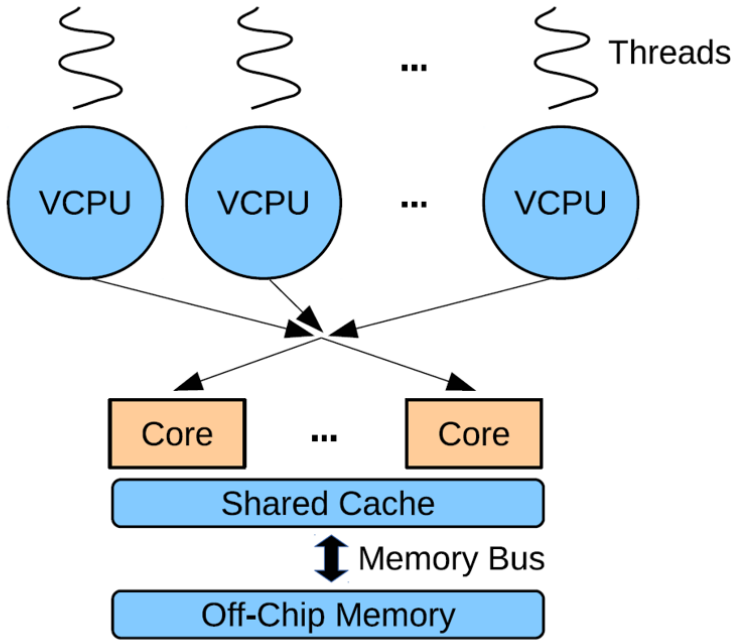

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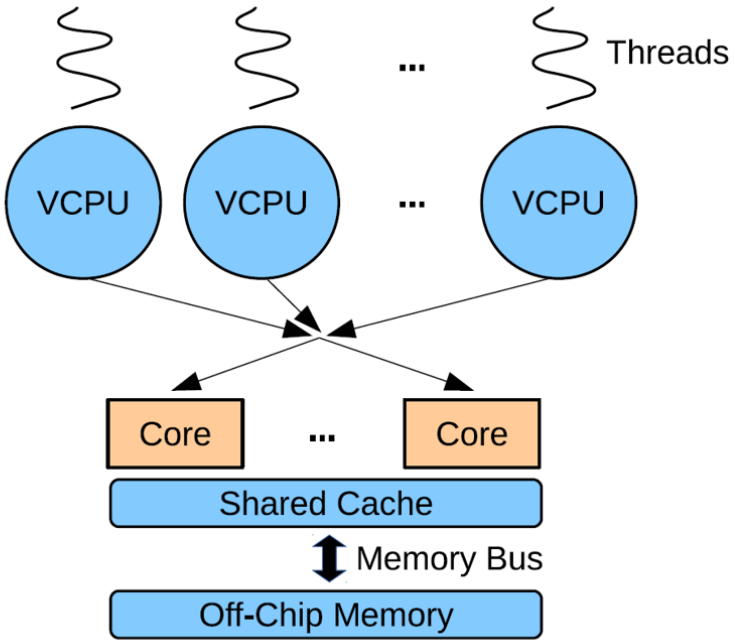
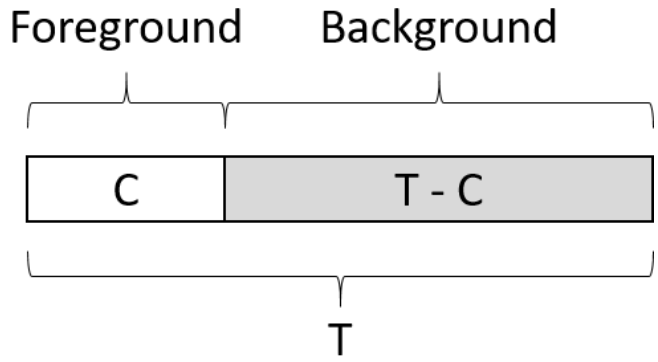
- Schedulability test $\sum_1^n(\frac{C_i}{T_i}) \leq n(\sqrt[n]{2}-1)$



Background Scheduling

- VCPU enters background mode upon depleting its budget (C)



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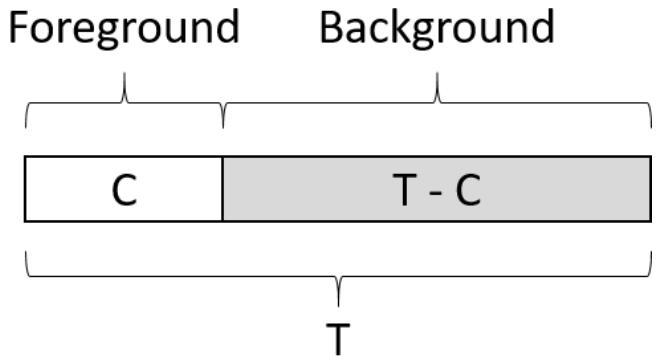

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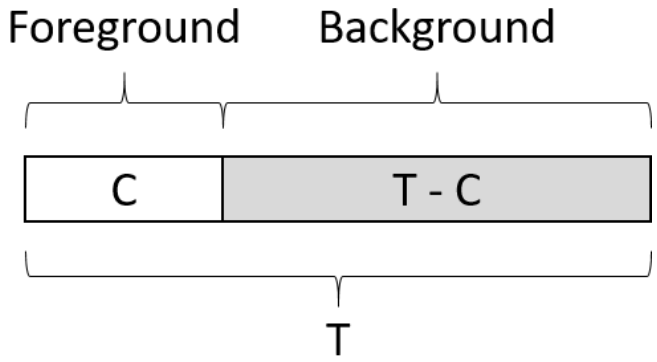

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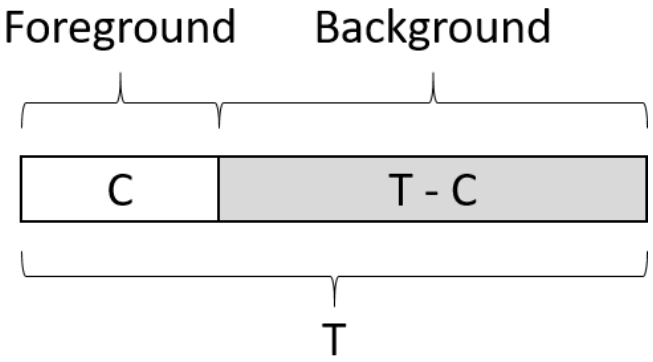

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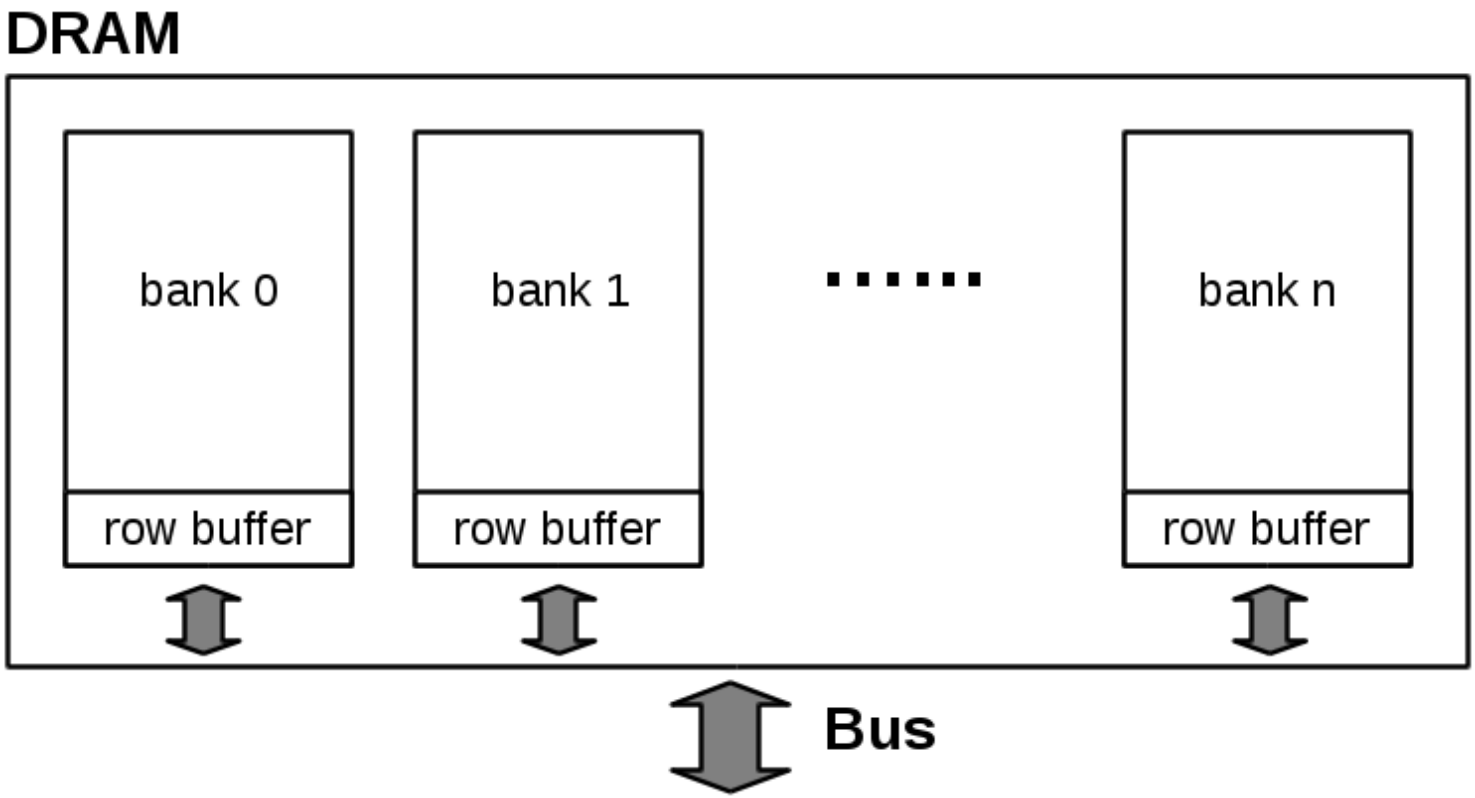
- Background CPU Time (**BGT**): time a VCPU runs when core in background mode
- Background scheduling: schedule VCPUs when core is in background mode
  - fair share of **BGT** amongst VCPUs on core

DRAM structure



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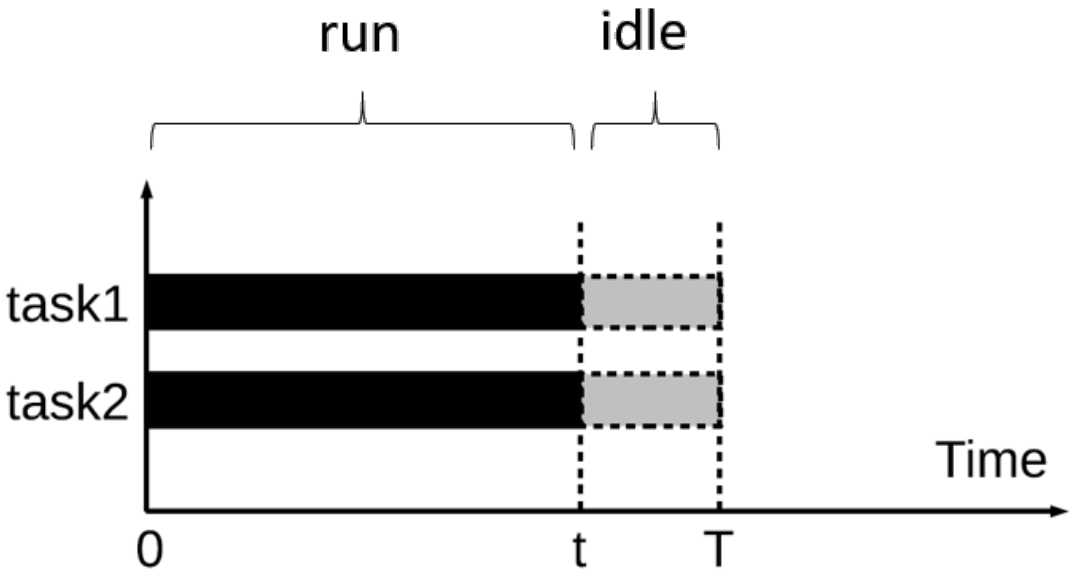

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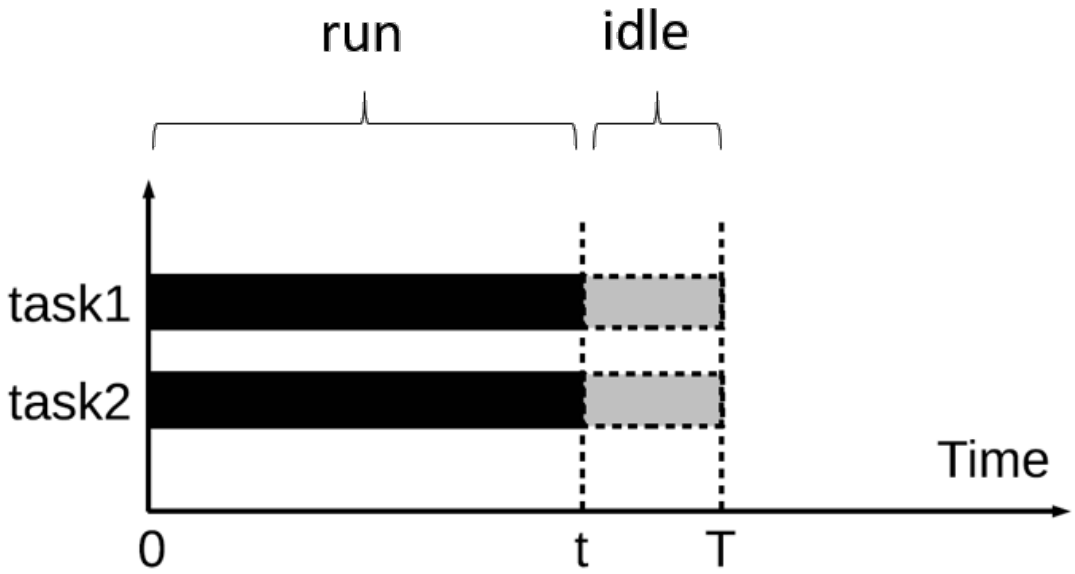
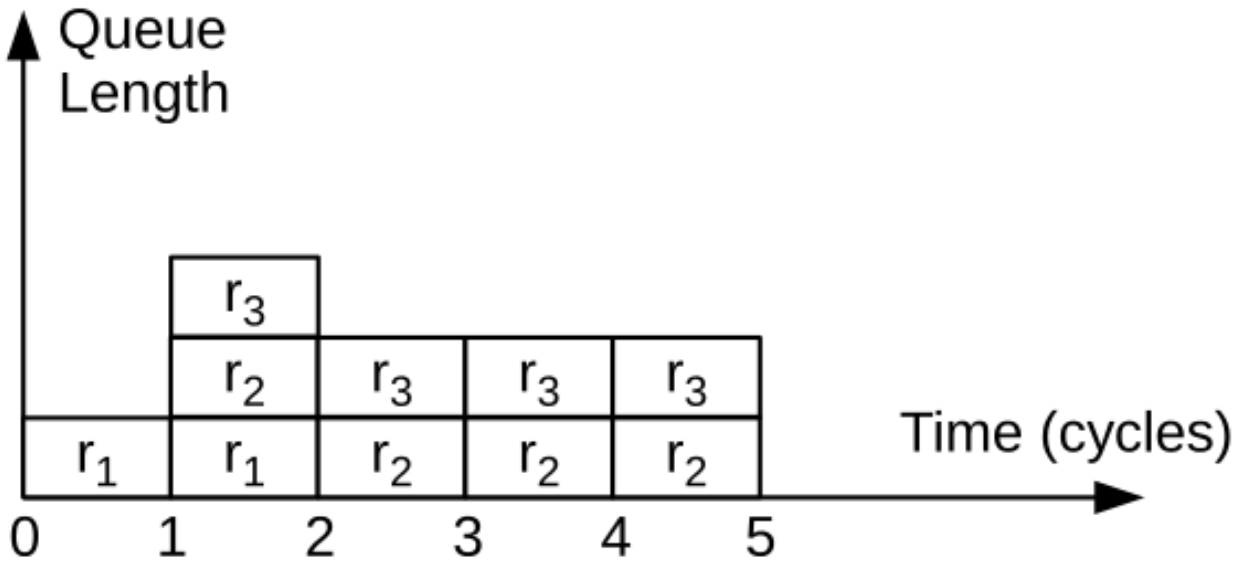


- Each task reduces its access rate by a factor of **(T-t)/T**
- Contention in [0, t] remains the same

Latency Metric



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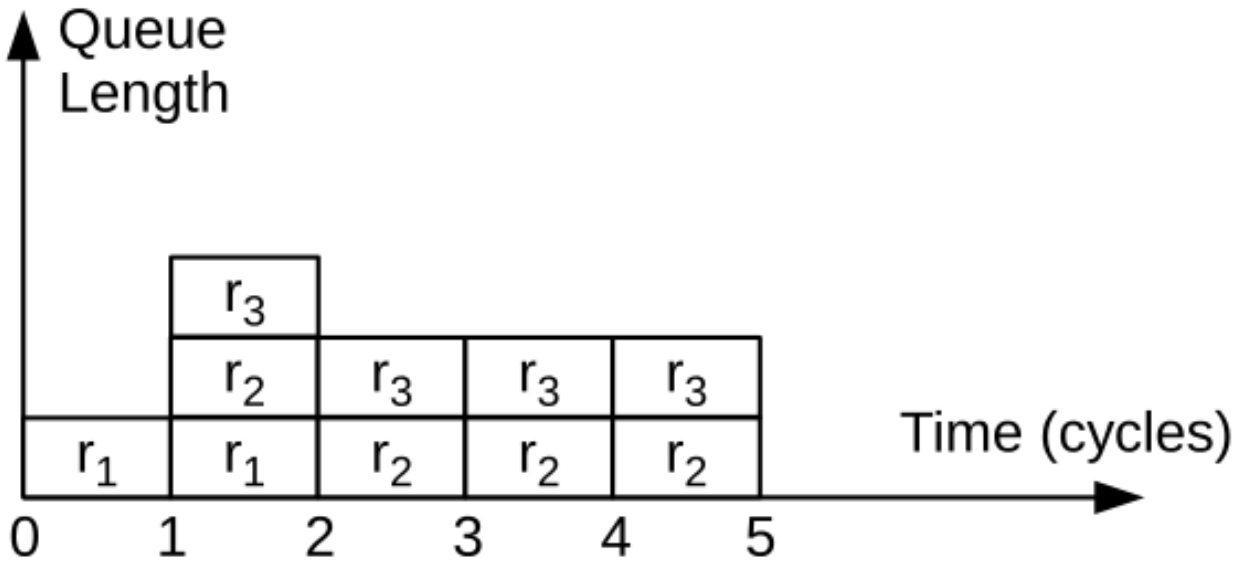

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Latency Metric

- UNC_ARB_TRK_REQUEST.ALL (**requests**): counts all memory requests going to the memory controller request queue
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- Average latency: $latency = \frac{occupancy}{requests}$

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- Proportional throttling
  - Every core is throttled at some point
  - Throttled time proportional to core's DRAM access rate

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- Only one migration thread active during a migration period
- Its execution of its entire capacity C does not lead to any other local VCPUs missing their deadlines
- Constraint on C:

$$C \geq 2 \times E_{lock} + E_{struct}$$

VCPU Load Balancing

- For every core, define Slack-Per-VCPU (**SPV**):

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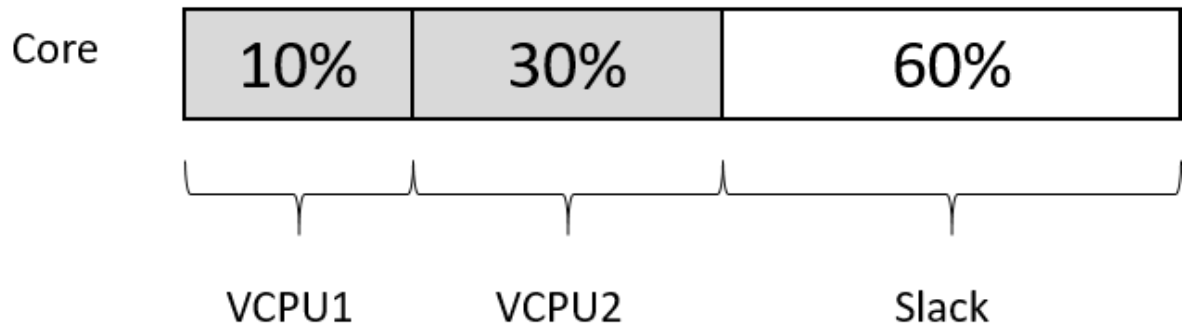

$$SPV = \frac{1-(10\%+30\%)}{2} = 30\%$$

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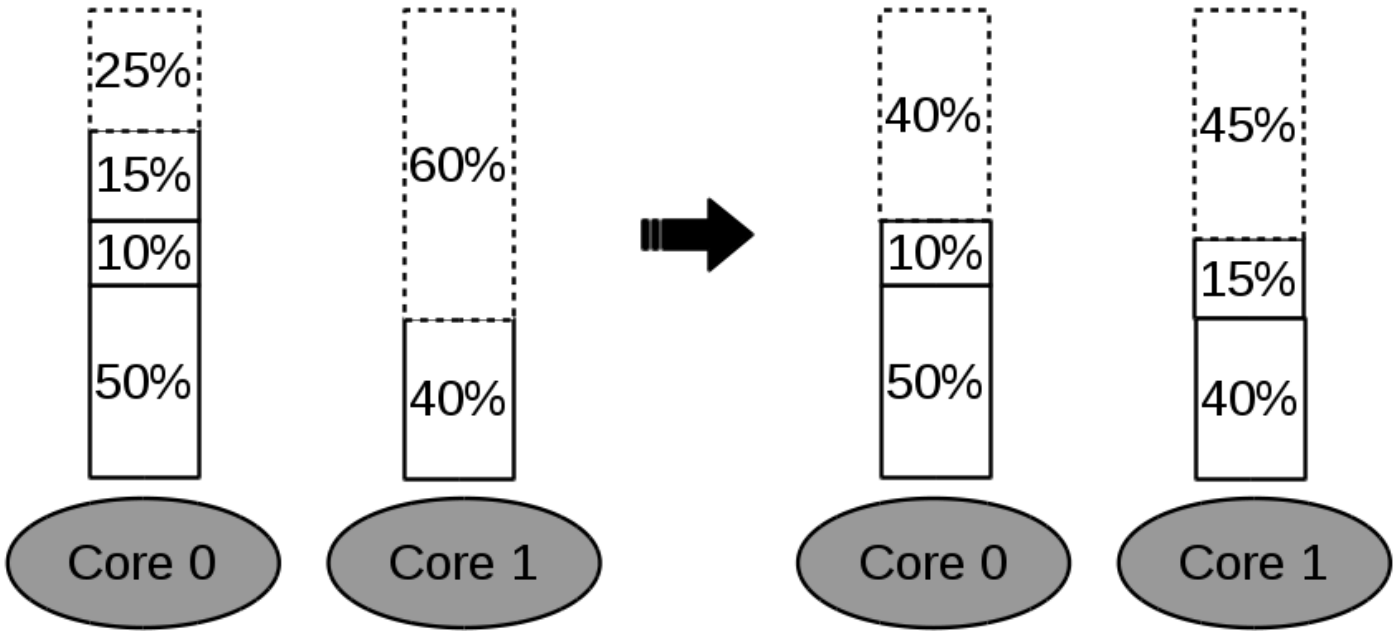

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- Extension of VCPU Load Balancing:
  destination core meets the cache requirement

Evaluation

- MARACAS running on the following hardware platform:

Processor	Intel Core i5-2500k quad-core
Caches	6MB L3 cache, 12-way set associative, 4 cache slices
Memory	8GB 1333MHz DDR3, 1 channel, 2 ranks, 8KB row buffers

Rate VS Latency

- Micro-benchmark m_jump:

```
byte array[6M];
for (uint32 j = 0; j < 8K; j += 64)
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- Each run, insert a different time delay in task1 and task2, task3 has no delay

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- Last column serves as reference, showing the **expected** performance of task3 using the corresponding thresholds

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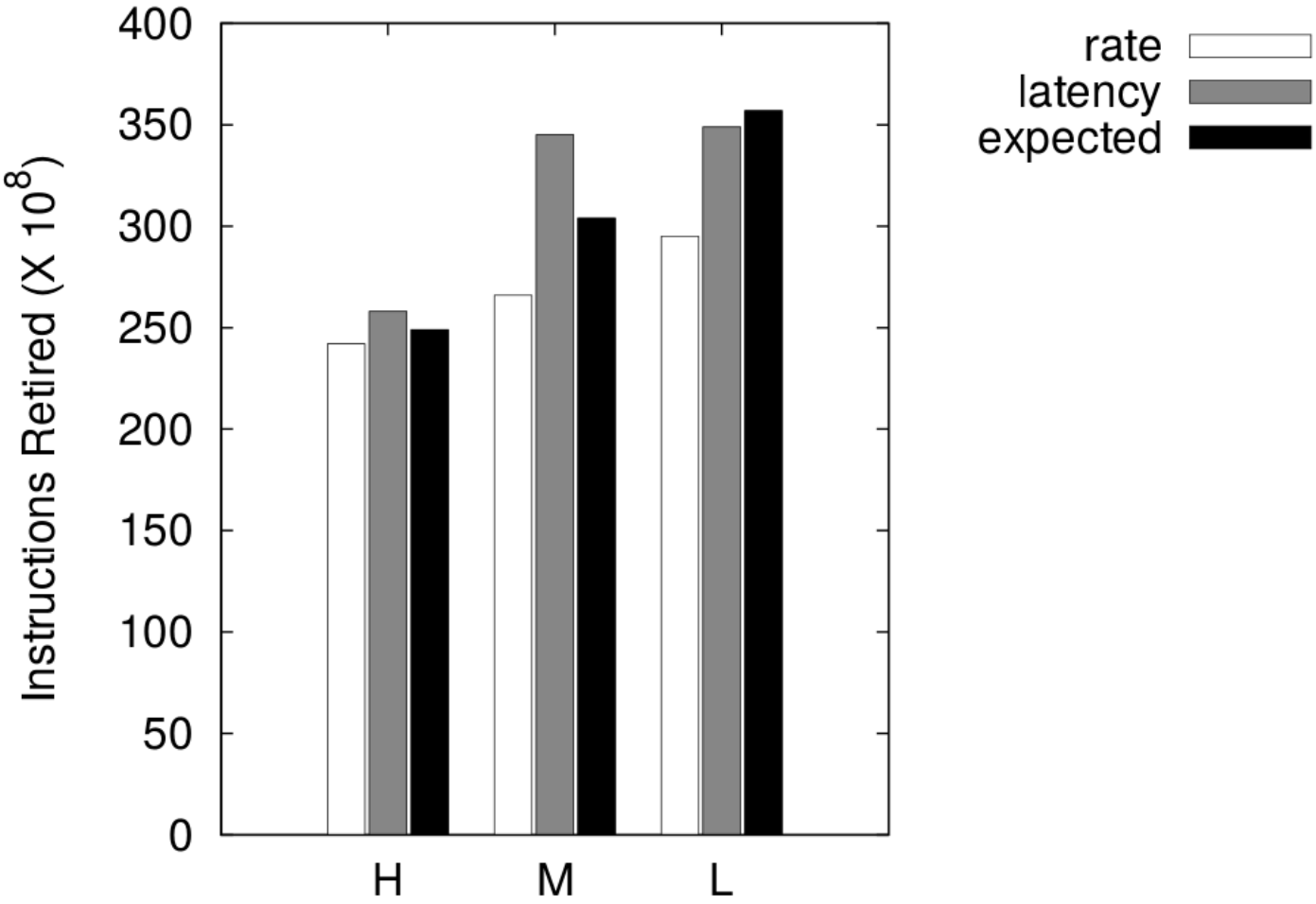

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- MARACAS fairly distributes background time across cores, for both fairness and better throttling