

Title: Simulation of Hardware Dynamic Scheduling on the DLX Architecture

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Abstract:

We describe our extension of the existing DLX simulator (DLXsim), available from the University of California at Berkeley, which allows the simulation of two hardware dynamic scheduling techniques. There are two DLXsim-like interactive simulators developed as part of this project. DLXscore simulates the operation of a DLX architecture equipped with scoreboard hardware. DLXscore provides the status of instructions, scoreboard tables, and statistics. DLXtomasulo simulates the operation of a DLX architecture equipped with a hardware implementation of Tomasulo's algorithm. DLXtomasulo provides the status of instructions, reservation stations, and statistics. Both programs allow the user to configure the number of functional units and the latency of floating point operations.

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URL = <http://cs-www.bu.edu/faculty/best/crs/cs550/yueh/dlxsim.html>