Boston University
College of Liberal Arts

Computer Science Department
111 Cummington Street, MCS 138
Boston, Massachusetts 02215
Tel: (617) 353-8919 / Fax: (617) 353-6457

CLA CS-450
Computer Architecture
Fall 1994

Meeting Place: MCS B29 **Meeting Time:** Tue & Thu (11:00am – 12:30pm)

Instructor: Prof. Azer Bestavros
- **Office:** MCS 276
- **Office Hours:** Thu 12:30pm – 2:00pm or by Email-arranged appointments
- **Email:** best@cs.bu.edu
- **Phone:** 353-9726

Textbook and References:

- *Computer System Architecture* Mano, Prentice Hall, Third Edition.
- *Computer Organization and Design: The Hardware/Software Interface* John Hennesy and David Patterson, Morgan Kaufmann Publishers Inc., 1993.
- *Computer Architecture: A quantitative approach* John Hennesy and David Patterson, Morgan Kaufmann Publishers Inc., Second Printing 1990.

Class participation:

- Class participation is vital for a full understanding and appreciation of the material to be covered. This must be complemented with a consistent and thorough reading of the assigned portions of the textbook for a given lecture.

Homeworks and Tests:

- There will be 8 homeworks and 2 problem sets throughout this class. You should expect one homework or problem set every week (or so). The purpose of homeworks will be to make sure that you are not "falling behind". They will not be difficult and most of the time will be straight out of the textbook. Homeworks will contribute 25% of your total grade. In addition to homeworks, you will be assigned Problem sets. These will be more elaborate, in that they will be more time consuming and might require coming up with designs, etc. Problem sets will be worth 15% of the course grade.
- There will be 3 quizes throughout the semester. The best 2 out of these will count for 20% of your grade. The final test will count for 40% of your grade.

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Syllabus

Class	Topic	Readings
9/13	Logic Circuits: Introduction to logic and VLSI circuits	1.1 - 1.2, 2.1
9/15	Logic Circuits: Boolean Algebra and combinational circuit design	1.3 - 1.5
9/20	Logic Circuits: Sequential circuit design	1.6 - 1.7
9/22	Logic Circuits: Computer building blocks	2.2 - 2.7
9/27	Data Representation: Basic computer arithmetic	3.1 - 3.3
9/29	Register Transfer Level: Basic microoperations	4.1 - 4.7
10/04	Quiz 1	
10/06	Datapath Design: Basics	5.1 - 5.5
10/13	Datapath Design: A basic computer	5.6 - 5.10
10/11	Datapath Design: Instruction Set Architecture	8.1 - 8.7
10/18	Controller Design: Basic Hardwired Control	
10/20	Controller Design: Basic Microprogrammed Control	7.1 - 7.3
10/25	Controller Design: Basic Microprogrammed Control	7.3 - 7.4
10/27	Controller Design: Microprogramming	
11/01	Quiz 2	
11/03	Pipelining and RISC processors	8.8
11/08	Pipelining and RISC processors	9.1 - 9.4
11/10	Pipelining and RISC processors	9.5
11/15	Memory system design and cashing	12.1 - 12.3
11/17	Cache Memory	12.5
11/22	Memory Management Hardware	12.6 - 12.7
11/24	Thanksgiving recess	
11/29	Multiprocessing: Interconnection structures and routing	13.1 - 13.4
12/01	Multiprocessing: Shared memory and cache coherence protocols	13.5
12/06	Slack	
12/08	Quiz 3	
12/13	Review	
12/20	Final Exam (12:30pm - 2:30pm)	

** Changes to this schedule will be announced if need be.*