Boston University
College of Liberal Arts

Computer Science Department
111 Cummington Street, MCS 138
Boston, Massachusetts 02215
Tel: (617) 353-8919 / Fax: (617) 353-6457

CLA CS-450
Computer Architecture
Fall 1995

Meeting Place: MCS B33 **Meeting Time:** Tue & Thu (11:00am – 12:30pm)

Instructor: Prof. Azer Bestavros
- **Office:** MCS 276
- **Office Hours:** Thu 2:00pm – 3:30pm or by Email-arranged appointments
- **Email:** best@cs.bu.edu
- **Phone:** 353-9726

Textbook and References:

- *Computer System Architecture* Mano, Prentice Hall, Third Edition.
- *Computer Organization and Design: The Hardware/Software Interface* John Hennesy and David Patterson, Morgan Kaufmann Publishers Inc., 1993.
- *Computer Architecture: A quantitative approach* John Hennesy and David Patterson, Morgan Kaufmann Publishers Inc., Second Printing 1990.

Class participation:

- Class participation is vital for a full understanding and appreciation of the material to be covered. This must be complemented with a consistent and thorough reading of the assigned portions of the textbook for a given lecture.

Homeworks and Tests:

- There will be approximately 8-10 homeworks throughout this class. You should expect one homework every week (or so). The purpose of homeworks will be to make sure that you are not "falling behind". They will not be difficult and most of the time will be straight out of the textbook, except for 2 homeworks which will be more elaborate, in that they will be more time consuming and might require coming up with designs, etc. Homeworks will contribute 40% of your total grade and will be weighed according to their difficulty level.
- There will be 2 quizes this semester. They will count for 20% of your grade. The final test will count for 40% of your grade.

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Syllabus

Class	Topic	Readings
9/05	First class meeting	
9/07	Review of Boolean Algebra and logic	1.1 - 1.2
9/12	Logic Circuits: Combinational circuit design	1.3 - 1.5
9/14	Logic Circuits: Sequential circuit design	1.6 - 1.7
9/19	Logic Circuits: Computer building blocks	2.2 - 2.7
9/21	VLSI technology: From silicon to a chip	
9/26	Data Representation: Basic computer arithmetic	3.1 - 3.3
9/28	Register Transfer Level: Basic microoperations	4.1 - 4.7
10/03	Datapath Design: Basics	5.1 - 5.5
10/05	Datapath Design: A basic computer	5.6 - 5.10
10/12	Datapath Design: Instruction Set Architecture	8.1 - 8.7
10/17	Controller Design: Basic hardwired controller design	
10/19	Controller Design: Basic microprogrammed Controller design	7.1 - 7.3
10/24	Controller Design: Microprogramming	7.3 - 7.4
10/26	Quiz #1 (in class from 11:00am to 12:30pm)	
10/31	Basic pipelined design of RISC processors	8.8
11/02	Dealing with data hazards in pipelined designs	9.1 - 9.4
11/07	Dealing with control hazards in pipelined designs	9.5
11/09	Advanced pipelining and superscalar processors	
11/14	Memory system design and caching	12.1 - 12.3
11/16	Cache Memory	12.5
11/21	Memory Management Hardware	12.6 - 12.7
11/28	Slack	
11/30	Quiz #2 (in class from 11:00am to 12:30pm)	
12/05	Multiprocessing: Shared memory and cache coherence protocols	13.5
12/07	Multiprocessing: Interconnection structures and routing	13.1 - 13.4
12/12	Review and conclusion	
12/18	Final Exam (12:30pm - 2:30pm)	

** Changes to this schedule will be announced if need be.*