Boston University
College of Arts and Sciences
Computer Science Department

111 Cummington Street, MCS
Boston, Massachusetts 02215
Web Home Page at http://www.cs.bu.edu
Tel: (617) 353-8919 / Fax: (617) 353-6457

CAS CS-450
Computer Architecture
Fall 1996

Meeting Place: MCS B23
Meeting Time: Tue & Thu (11:00am – 12:30pm)
Web Home Page: `http://www.cs.bu.edu/~best/crs/cs450`

Instructor: Prof. Azer Bestavros
- ⋄ **Office:** MCS 276
- ⋄ **Office Hours:** Mon 3:00pm – 4:30pm or by Email-arranged appointments
- ⋄ **Email:** best@cs.bu.edu
- ⋄ **Phone:** 353-9726

Overview:
The performance of computing systems is dramatically influenced by how well software designers understand the basic hardware techniques at work in the system. Similarly, hardware designers must clearly understand the effects of their work on software applications. Our emphasis by the end of this course is to undertand the relationship between hardware and software and to focus on the concepts that are the basis for modern computers. But, to be able to reach that goal, we must first understand what goes into a computer's architecture!

Computers are built as a hierarchy of "interpretation and control" abstractions. At the bottom, we start with circuit design, and we proceed to logical design, datapath, control unit and I/O design, instruction set design, compiler, operating system, and applictaions. Computer Architecture, the subject of this course, refers to the coordination of these various levels of abstractions—How to get them all to work together to achieve the best performance.

In the first part of this course, we will start with the basics: how to implement the computer's building blocks using the most basic electronic components, namely transistors and capacitors. Next, we will understand how VLSI technology can integrate our building blocks efficiently. In that respect, we will go through the design of a simple computer by putting together its datapath (ALU, registers, and buses), and its control unit.

In the second part of this course, we will move up in the hierarchy of "interpretation and control" abstractions and examine the aspects that go into the design of a computer's instruction set. In that regard, we will contrast (with the help of case studies) the two predominant philosophies in instruction set design, RISC and CISC, and we will understand the impact of such designs on compiler and operating system.

In the third part of this course, we will look at various optimization techniques that could improve the performance of our simple computer. This includes pipelining, caching, and multiprocessing. Also, we will examine networking technologies, including the TCP/IP stack, which enable the construction of networked distributed computing systems.

At the end of this course—and if the experience of other students who took this course before is any indication—your outlook on computers and how they work will change once and for all because you will be able to understand what *really* happens when your computer executes that simple C program of yours! I hope you enjoy taking this class as much as I enjoy teaching it ☺

Textbook and References:

- *Computer System Architecture* Mano, Prentice Hall, Third Edition.
- *Computer Organization and Design: The Hardware/Software Interface* John Hennesy and David Patterson, Morgan Kaufmann Publishers Inc., 1993.
- *Computer Architecture: A quantitative approach* John Hennesy and David Patterson, Morgan Kaufmann Publishers Inc., Second Edition 1995.

Class participation:

- Class participation is vital for a full understanding and appreciation of the material to be covered. This must be complemented with a consistent and thorough reading of the assigned portions of the textbook for a given lecture.

Homeworks and Tests:

- There will be approximately 8 homeworks throughout this class. You should expect one homework every week (or so). The purpose of homeworks will be to make sure that you are not "falling behind". They will not be difficult and most of the time will be straight out of the textbook, except for 2 homeworks which will be more elaborate, in that they will be more time consuming and might require coming up with designs, etc. Homeworks will contribute 40% of your total grade and will be weighed according to their level of difficulty.
- There will be a midterm exam on November 5th. This exam will count for 20% of your grade. The final test will count for 40% of your grade.

Policy on Collaboration:

- There is nothing wrong in principle about discussing the topics covered in the course with your peers. However, there are severe consequences to presenting their work as if it were yours (*e.g.*, copying their homework solutions, or not acknowledging their help if main ideas about homework solutions were communicated orally). This is nothing less than **plagiarism** and will be punished accordingly.

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Syllabus

Class	Topic	Readings
9/03	Review of Boolean Algebra and Logic	1.1 - 1.2
9/05	Combinational Logic Circuit Design	1.3 - 1.5
9/10	Sequential Logic Circuit Design	1.6 - 1.7
9/12	Computer Building Blocks	2.2 - 2.7
9/17	VLSI technology	
9/19	Data Representation and Basic Computer Arithmetic	3.1 - 3.3
9/24	Register Transfer Level and Basic Microoperations	4.1 - 4.7
9/26	Datapath Design Basics	5.1 - 5.5
10/01	Datapath Design of a Basic Computer	5.6 - 5.10
10/03	Instruction Set Architecture	8.1 - 8.7
10/08	Basic Hardwired Controller Design	
10/10	Basic Microprogrammed Controller Design	7.1 - 7.3
10/17	Microprogramming	7.3 - 7.4
10/22	Basic Pipelined Design of RISC Processors	8.8
10/24	Dealing with Data Hazards in Pipelined Designs	9.1 - 9.4
10/29	Dealing with Control Hazards in Pipelined Designs	9.5
10/31	Pipelining Review	
11/05	Quiz #1 (in class from 11:00am to 12:30pm)	
11/07	Advanced Pipelining and Superscalar Processors	
11/12	Memory System Design and Caching	12.1 - 12.3
11/14	Cache Memory	12.5
11/19	Memory Management Hardware	12.6 - 12.7
11/21	Shared Memory and Cache Coherence Protocols	13.5
11/26	Interconnection Structures and Routing	
12/03	Internetworking and TCP/IP basics	
12/05	Slack	
12/10	Review and Conclusion	
12/18	Final Exam (12:30pm - 2:30pm)	

** Changes to this schedule will be announced if need be.*