Boston University
College of Liberal Arts

Computer Science Department
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CLA CS-550
Advanced Computer Architecture
Spring 1994

Meeting Place: MCS B-31 **Meeting Time:** Tue & Thu (9:30am – 11:00pm)

Instructor: Azer Bestavros
- ◇ **Office:** MCS-276
- ◇ **Office Hours:** Thu 11:00 – 12:30pm, or by appointments arranged through Email
- ◇ **Email:** best@cs.bu.edu
- ◇ **Phone:** 353-9726

Textbook and References:

- ◇ *Computer Architecture: A quantitative approach* John Hennesy and David Patterson, Morgan Kaufmann Publishers Inc., Second Printing 1990.
- ◇ *High-Performance Computer Architecture* Stone, Addison Wesley., Third Edition.
- ◇ *Computer System Architecture* Mano, Prentice Hall, Third Edition.
- ◇ *A collection of papers from various journals and conference proceedings – to be distributed.*

Class participation:

- ◇ Class participation is vital for a full understanding and appreciation of the material to be covered. This must be complemented with a consistent and thorough reading of the assigned portions of the textbook for a given lecture.

Homeworks and Tests:

- ◇ There will be a number of homeworks (≈ 6) spread out throughout the course. Some will be short and direct (one-week homeworks); others will be long and more like design projects (two-week homeworks).
- ◇ In addition to the homeworks there will be a final exam.

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Syllabus

Class	Topic	Readings
1/18	First class meeting: Motivation and Overview	
1/20	Introduction: Key principles & terminology	Ch.1
1/25	Performance and Cost: Measures and Evaluation	Ch.2
1/27	Instruction Set Design: A review of basic principles	Ch.3
2/01	Instruction Set Design: Evaluation of alternatives	Ch.3
2/03	Instruction Set Design: Relationship with software technology	Ch.3
2/08	Instruction Set Design: Case Studies (VAX, IBM 360/70, 8086 & DLX)	Ch.4
2/10	Instruction Set Design: Conclusion	Ch.4
2/15	Processor Design: Building blocks	Mano
2/17	Processor Design: From N-P Junctions to Logic Circuits	
2/22	No Class. (Substitute Monday)	
2/24	Processor Design: Datapath and Control	Ch.5
3/01	Processor Design: Hardwired and Microprogramming control	Ch.5
3/03	Processor Design: Conclusion	Ch.5
3/08	Spring Recess	
3/10	Spring Recess	
3/15	Pipelining: Introduction and concept	Ch.6
3/17	Pipelining: Basic designs	Ch.6
3/22	Pipelining: Dynamic scheduling & Parallelism	Ch.6
3/24	Pipelining: Conclusion	Ch.6
3/29	Vector Processing	Ch.7
3/31	Memory-hierarchy design: Basic concepts	Ch.8
4/05	Memory-hierarchy design: Caching	Ch.8
4/07	Memory-hierarchy design: Main and virtual memory	Ch.8
4/12	Input Output design	Ch.8
4/14	Parallel Processing: Introduction	Ch.10
4/19	Parallel Processing: Interconnection Topologies	Papers
4/21	Parallel Processing: Hypercube and Butterfly Machines	Papers
4/26	Parallel Processing: Dataflow and Shared-Memory Machines	Papers
4/28	Parallel Processing: Message-Passing and SIMD Machines	Papers
5/03	Conclusion	
5/05	Take-home final exam due	

** Changes to this schedule will be announced if need be.*