Estimated time: 1 hour Closed book/notes exam	**DWE: Systems / Fall 1992** **Computer Architecture**	Prof: Azer Bestavros Email: best@cs.bu.edu

Answer ONLY TWO of the following three EQUAL-WEIGHT questions

State any asumptions clearly

1 A computer system has the following features:

a. 90% of all memory accesses are found in the cache;
b. Each cache block is 2 words and the whole block is read on any miss;
c. The processor sends references to its cache at the rate of 10^7 words per second;
d. 25% of the references in (c.) are writes;
e. Assume that the bus can support 10^7 words per second, reads or writes;
f. The bus reads/writes a single word at a time; It cannot read/write two words at once;
g. Assume that at any point in time 30% of the blocks in the cache have been modified;
h. The cache allocates a block on a write miss.

You are considering adding a peripheral to the bus of the system described above, and you want to know how much of the bus bandwidth is already used. Calculate the percentage of bus bandwidth (*traffic ratio*) used on the average in the two cases below.

a. The cache is write through.
b. The cache is write back.

2

a. Explain briefly the "Scoreboarding" and the "Tomasulo" algorithms for dynamic scheduling of pipelines.
   1. What kinds of Hazards does each one of these techniques avoid?
   2. What kinds of Hazards does each one of these techniques treat? How?

b. Program reference patterns are used extensively to design higher performance architectures. Explain briefly what is meant by *spacial* & *temporal* locality of reference.
   1. Explain how spacial locality can be used to design fast memories,
   2. Explain how temporal locality can be used to reduce pipeline branch penalty.

3 One technique that tries to get the best of both the worlds of vertical and horizontal microarchitectures is a two-level control store, which tries to combine small control-store size with wide instructions stored in *Nanocode memory.* The idea is to have a large number of vertical microinstructions point to a few unique horizontal nanoinstructions. Consider a computer with M microinstructions, where each is a bits wide. Also, let N be the size of the nanostore, which has b bit wide nanoinstructions.

a. Contrast *Hardwired* and *Microprogrammed* control.

b. Contrast *Horizontal* and *Vertical* Microprogrammed control.

a. Find a general rule to establish the conditions under which the two-level control store described above uses fewer bits than a single-level control store?

b. Would a 3-level control store have any advantages over a 2-level control store? Explain.

Good Luck