Estimated time: 90 mins Closed book/notes exam	**DWE: Systems / Fall 1993** **Computer Architecture**	Prof: Azer Bestavros Email: best@cs.bu.edu

Answer the following TWO EQUAL-WEIGHT questions

State any asumptions clearly

1

a. An n-dimentional Cube Connected Cycle is a Hypercube where each node is replaced with a "ring" (cycle) consisting of n nodes, where n is the dimension of the Hypercube. What is the total number of nodes in a Cube Connected Cycle of dimension n ? What is the diameter? Suggest an algorithm for routing in a Cube Connected Cycle.

b. Explain briefly the function of the *branch target buffer* and the *steps* involved in handling an instruction with a branch-target. Which property should be present for a program to capitalize on a branch target buffer?

c. Explain briefly the services provided by the various layers of the ISO/OSI reference model? Which layer is responsible for providing a reliable transmission abstraction? Which layer is responsible for network congestion control?

d. *Software pipelining* and *trace scheduling* are two techniques often used by compilers of *super-scalar processors*. What is meant by a super-scalar processor? Explain briefly and contrast both software pipelining and trace scheduling techniques.

e. Explain what is meant by *bypassing* in pipelined design. What kind of hazard does bypassing deal with? Given a n-stage pipelined design and a load-store ISA with 3 operands (e.g. DLX), estimate the complexity (as a function of n) of the bypass circuitry.

2

a. Explain briefly the difference between *fully associative* and *direct mapping* cache organizations.

1. Give an example of a memory reference pattern in which a direct mapping cache organization consistently outperforms a fully associative one.
2. Give an example of a memory reference pattern in which a fully associative cache organization consistently outperforms a direct mapping cache organization.

Assume LRU replacement strategy.

b. The base CPI of a pipelined processor (assuming a perfect memory system) is 1.5. What is the CPI if the following cache organizations are used? (see Table-1)

1. Direct-mapped, 16-KB unified cache using write back.
2. 2-way-set-associative, 16-KB unified cache using write back.
3. Direct-mapped, 32-KB unified cache using write back.

Assume that memory latency is 6 clocks, the transfer rate is 4 bytes per clock cycle and that 50% of the transfers are dirty. There are 16 bytes per block and 20% of the instructions are data-transfer instructions. The caches fetch words of the block in address order and the CPUs stall until all words of the block arrive. There are no write buffer. There is a TLB that takes 20 clock cycles on a TLB miss and doesn't affect performance on a TLB hit. Assume that 1% of all references aren't found in the TLB, either when addresses come directly from the CPU or from a cache miss.

4. What is the impact on performance of the TLB if the cache above is physical or virtual?

Good Luck