Estimated time: 90 mins Closed book/notes exam	**DWE: Systems / Fall 1994** **Computer Architecture**	Prof: Azer Bestavros Email: best@cs.bu.edu

Answer the following questions

State any asumptions clearly

1

a. Two machines (I & II) executed a hypothetical benchmark program. Machine I was clocked at 5 MHz, executed 1 MIPS, with a CPU time of 12x seconds. Machine II was clocked at 25 MHz, executed 18 MIPS, with a CPU time of 1x seconds. Which of the two machines would you guess to be a RISC architecture? and which one would you guess to be a CISC architecture? Why? [10%]

b. Suppose that we have 16 memory banks with an access time of 12 clocks. How long would it take to complete a 64-element vector load with a stride of 1? With a stride of 32? [10%]

c. An Omega network is a multi-stage switching network where each stage is composed of a perfect-shuffle and a set of 2x2 crossbars. Draw a diagram for a 16-node Omega network. What is the bisection width of the network? Suggest an algorithm for routing in an N-node Omega network. [15%]

d. Explain briefly the function of the *translation-lookaside buffer* and the *inverted page table* in the design of a virtual memory system. [15%]

2

a. In order to obtain a zero-delay branch for a pipelined machine, a modified branch-target buffer design has been suggested. The buffer simply caches the target instruction rather than the target PC. On a branch that hits in the branch-target buffer, the target instruction is fetched and sent to the pipeline in place of the branch instruction itself! Assume that the base CPI is 1, that a 90% hit rate in the branch-target buffer is achieved, that a 87% prediction accuracy is achieved, that the misprediction penaly is 4 cycles, that the buffer miss penaly is 3 cycles, that 2% of all instructions are unconditional branches, and that 11% of all instructions are conditional branches. What is the CPI of this machine <u>with</u> and <u>without</u> the zero-delay branch modification? Show all calculations. [25%]

b. A bus-connected multiprocessor has 16 processors, each connected to an on-board private cache which is connected to a common bus. Globally shared memory is also connected to the bus. The private cache and the shared memory form a two-level access hierarchy. Each processor is rated with 10 MIPS if a 100% cache hit ratio is assumed. On the average, each instruction needs 0.2 memory access. The read access and write access are assumed equally probable. For a crude approximation, consider only the penalty caused by shared-memory access and ignore all other overheads. The cache is targeted to maintain a hit ratio of 0.95. A cache access on a read-hit takes 20ns; that on a write-hit takes 60ns with a write-back scheme, and with a write-through scheme it needs 400ns. When a cache block is to be replaced, the probability that it is dirty is estimated as 0.1. An average block transfer time between the cache and shared memory via the bus is 400ns. Answer the following questions: [25%]

- ◇ Derive the effective memory-access times per instruction for the write-through and write-back caches separately.
- ◇ Calculate the effective MIPS rate for each processor under write-through and write-back caches. Determine the tightest upper bound on the effective MIPS rate of the 16-processor system under both policies.

Good Luck