Estimated time: 90 mins Closed book/notes exam	**DWE: Systems / Fall 1995** **Computer Architecture**	Prof: Azer Bestavros Email: best@cs.bu.edu

Answer the following questions

State any asumptions clearly

a. What is the number of nodes in a n-dimensional Cube-Connected-Cycle? Assuming unidirectional connections, what is the diameter of this topology? [10%]

b. What are the different stages of a pipelined processor design that uses scoreboarding for dynamic scheduling? Which of these stages require the instructions to pass through "in order" and which ones allow the instructions to pass through "out of order". [15%]

c. Consider a 5-stage pipelined CPU (with NO bypassing circuitry), which has the following stages: Instruction Fetch (IF), Decode and Read operands from registers (DR), Execute (EX), access MEMmory (MEM), and Write Back results in registers (WB). Furthermore, assume that the probability of a Read-After-Write hazard between instruction i and instruction *i-1, i-2, i-3, i-4* is *0.1, 0.04, 0.02, 0.005*, respectively. Ignoring all other hazards, compute the expected speedup of this pipeline. Compare this to the ideal speedup. [15%]

d. Suppose we have a deeply pipelined machine, for which we implement a branch-target buffer for conditional branches only. Assume that the misprediction penalty is always 4 cycles, that the buffer miss penalty is always 3 cycles, and that the hit rate in the buffer is 90%. **What should be the accuracy of the prediction mechanism for the machine with the branch target buffer to outperform a machine with a fixed 2-cycle branch penalty?** Assume that the base CPI without branch stalls is 1 and that 11% of all instructions are conditional branches. [20%]

e. You are asked to evaluate a proposed change to the ISA of a machine (call it machine X), which is not pipelined and has a load/store ISA with the following instruction mix and performance characteristics:

Class of Operation	Frequency	Clock cycle count
ALU operations	43%	1
Loads	21%	2
Stores	12%	2
Branches	24%	2

Upon further experimentation, it was determined that 25% of the ALU operations directly use a loaded operand that is not used again. In other words, the operand is loaded from memory, used in one ALU instruction and then not used again. This observation led to suggesting an alternative machine design (call it machine Y). The ISA of machine Y is identical to that of machine X, except that a new class of register-memory ALU instructions is included to allow combining a load and an ALU operation. The new class of operations has a clock cycle count of 2. For all other classes of instructions, the clock cycle count is increased by 1. The clock cycle time for Y is the same as that of X. **Would you recommend changing the design from machine X to machine Y? Why and why not.** [20%]

f. You are to choose the organization of an instruction-only cache to be used in the CPU of a batch system and you are presented with two alternatives:
   - ◇ A direct-mapped 64-byte cache memory, or
   - ◇ A 4-way set associative 64-byte cache memory with LRU replacement.

Which one of these alternatives would you choose? and why? Assuming that each instruction is 2 bytes long, and that the cache is "cold", what would be the hit rate achievable by the organization that you choose when the following code segment (to add a scalar to a 16-element vector) is executed? [20%]

```
      LW R1, #128        % Load the offset (length of vector)
Loop: LD F0, 0(R1)       % Load an element from the vector at base address = 0
      ADDD F4, F0, F2    % Add the scalar in F0 to the vector element
      SD 0(R1), F4       % Store the vector element back
      SUB R1,R1,#8       % Decrease the offset by the length of 1 element
      BNEZ R1, Loop      % Until no more!
```

Good Luck