Estimated time: 90 mins Closed book/notes exam	**DWE: Systems / Fall 1997** **Computer Architecture**	Prof: Azer Bestavros Email: best@cs.bu.edu

Answer ALL Questions

State any asumptions clearly

a. Explain briefly how the Tomasulo algorithm for dynamic scheduling of pipelines deals with the WAW hazards. [5]

b. Write down an expression for the average latency of a memory access in a system with n levels of caches: $L_1, L_2, \ldots L_n$. Assume that the miss rate for L_i is r_i and that the hit time for L_i is t_i. [5]

c. Explain what is meant by (1) strip mining, and (2) chaining in Vector Processing. Give vector code segments that illustrate the use of these techniques. [10]

d. Cache misses are categorized into compulsory misses, capacity misses and conflict misses. Briefly define each one of these categories. Explain the effect of (1) overall cache size, (2) line size, and (3) associativity on each of these categories. [10]

e. How many leaf nodes could be connected using an n-dimensional k-ary Mesh Of Trees (MOT)? What is the diameter of such topology? What is the average number of hops between two leaf nodes selected at random from a MOT? [10]

f. A pipelined CPU that uses the Tomasulo algorithm and a blocking cache memory system has a CPI of 0.6. Simulation studies of a number of benchmarks indicate that: 70% of all cache accesses experience no blocking, 20% wait for 1 previous miss to be resolved, 8% wait for 2 previous misses, and 2% wait for 3 or more previous misses. Assuming that the average number of memory operations per instruction is 0.25 and that the average blocking time is 2 cycles, what are the performance implications of replacing the above blocking cache memory system with a non-blocking "hit under i miss" cache memory system, for $i = 1, 2, 3, \ldots, \infty$. Assume that the clock cycle has to increase by $5i\%$ to accomodate the non-blocking "hit under i miss" cache memory system. What value of i would you pick (assuming cost is not an issue)? [20]

g. You are given a 2-digit Binary-Coded Decimal (BCD) number. The most significant digit of the BCD number is stored in bits $a_3\ a_2\ a_1\ a_0$ and the least significant digit of the BCD number is stored in bits $b_3\ b_2\ b_1\ b_0$. Show the schematic design of a logical circuit that converts this 2-digit BCD number into a 7-bit binary number $c_6\ c_5\ c_4\ c_3\ c_2\ c_1\ c_0$. Assume that only the following components are available for your use AND, OR, and NOT gates. [15]

h. Two improvements are implemented to improve the design of a scalar *5-stage pipelined* computer system. The first reduces the branch miss penalty from 2 clock cycles to 1 clock cycle through the use of a branch target buffer. The second reduces the data cache miss penalty from 4 clock cycles to 2 clock cycles. Assume that the hit rate of a typical workload is 95%, that 30% of all instructions are load/store, that 20% of all instructions are branches, that the branch target buffer miss rate is 8% and that its misprediction rate is 20%. Except for the cache and branch hazards, you could assume that all other entanglements are resolved with no penalty. What is the CPI of this improved machine? [15]

i. A parallel computer consists of 32 processors, each with a CPI of 1 and a clock cycle of 10 nanoseconds. Assuming that all references to local memory are served from the cache (i.e. in 1 clock cycle) and that all references to remote memories are blocking and have a latency of 2,000 nanoseconds. What is the speedup for this 32-processor computer assuming that 1% of all instructions involve a remote reference. [10]