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DWE: Architecture

Syllabus

1. **Preliminaries:**
   a. Representation of information and coding techniques.
   [Mano: Chapter 3].
   b. Integer/floating-point arithmetic and logic operations.
   [Mano: Chapter 10], [Stallings: Chapter 7], [P&H-1: Appendix-A], [P&H-2: Chapter 4].
   c. Combinational and sequential circuit design; VLSI preliminaries.
   [Mano: Chapters 1,2].
   d. Cost and performance metrics.
   [P&H-1: Chapter 2], [P&H-2: Chapter 2], [Stone: Chapter 1].
2. **Instruction Set Architecture:**
   a. Classification/choices based on number of operands, addressing modes, and data types; GPR ISA.
   [P&H-1: Chapter 3], [P&H-2: Chapter 3], [Mano: Chapter 8], [Stallings: Chapters 8,9].
   b. RISC versus CISC; Effect of optimizing compilation.
   [P&H-1: Chapter 3], [Stallings: Chapter 13].
   c. Case studies and Measurements.
   [P&H-1: Chapter 4, Appendix B, C, D, E].
3. **Basic Processor Implementation:**
   a. Datapath design.
   [P&H-1: Chapter 5], [P&H-2: Chapter 5], [Stallings: Chapters 10], [Mano: Chapter 5].
   b. Control unit; hardwired vs. microprogrammed control; Microprogramming.
   [P&H-1: Chapter 5], [P&H-2: Chapter 5], [Stallings: Chapters 11,12], [Mano: Chapter 7].

3. **Memory and I/O:**

   a. Technologies; hierarchy; Cache memory; Virtual memory; Memory management hardware.
   [P&H-1: Chapter 8], [P&H-2: Chapter 7], [Stallings: Chapters 4], [Mano: Chapter 12], [Stone: Chapter 2].

   b. I/O organization; Mapped I/O vs. Channels.
   [P&H-1: Chapter 9], [P&H-2: Chapter 8], [Stallings: Chapters 5], [Mano: Chapter 11].

5. **Pipelining:**

   a. In-order basic datapath pipelining; Structural hazards; Data hazards; Control hazards.
   [P&H-1: Chapter 6], [P&H-2: Chapter 6], [Mano: Chapter 9].

   b. Advanced pipelining techniques; Bypassing; Scoreboarding; Tomasulo's Algorithm; Branch target buffer.
   [P&H-1: Chapter 6], [P&H-2: Chapter 6], [Mano: Chapter 9], [Stone: Chapter 3].

6. **Super Scalar and Vector Processors:**

   a. Super-scalar architectures; VLIW; Impact on Compiler technology.
   [P&H-1: Chapter 6], [P&H-2: Chapter 6], [Stallings: Chapter 14].

   b. Vector Processing.
   [P&H-1: Chapter 7], [P&H-2: Chapter 7], [Mano: Chapter 9], [Stone: Chapter 5].

7. **Parallel Architectures:**

   a. Flynn Classification; Basic SIMD, MISD, MIMD, Dataflow, designs; Synchronous vs. Asynchronous; Message passing vs. Shared memory.
   [P&H-1: Chapter 10], [P&H-2: Chapter 9], [Mano: Chapter 13], [Stallings: Chapter 15].

   b. Interconnection networks and topology; Bus, Ring, Crossbar, Meshes, Shuffle exchanges and Butterflies, MOTs, Hypercubes, Fetch-and-op combining networks.
   [Stone: Chapter 6]

References

[P&H-1] *Computer Architecture: A quantitative approach* (Second Printing), John Hennesy and David Patterson, Morgan Kaufmann Publishers Inc., 1990.

[P&H-2] *Computer Organization and Design: The Hardware/Software Interface*, John Hennesy and David Patterson, Morgan Kaufmann Publishers Inc., 1993.

[Stone] *High-Performance Computer Architecture* (Third Edition), Harold Stone, Addison Wesley, 1992.

[Mano] *Computer System Architecture* (Third Edition), Mano, Prentice Hall, 1992.

[Stallings] *Computer Organization and Architecture: Principles of Structure and Function* (third edition), William Stallings, Macmillan, 1993.

[Tanenbaum] *Structured Computer Organization* (third edition), Prentice Hall, 1990.