CMOS LIMITING OPTICAL PREAMPLIFIERS USING DYNAMIC BIASING FOR WIDE DYNAMIC RANGE

Sharon Goldberg, Stephen Liu, Sean Nicolson and Khoman Phang

Department of Electrical and Computer Engineering, University of Toronto, Toronto, Ontario, M5S 3G4, Canada
Email: sharon.goldberg@utoronto.ca

ABSTRACT

This paper presents limiting techniques for improving the dynamic range of CMOS optical preamplifiers while minimizing power dissipation. A fully-differential transimpedance amplifier using diodes clamps to limit output voltage is analyzed. A design with a transimpedance gain of 5kΩ and total bias current of 2.9mA is simulated handle a maximum photocurrent of 400μA at 100Mbps, with an input-referred noise of 177nA(rms). Dynamic biasing techniques are then introduced to improve dynamic range. A Class A topology is simulated to double maximum photocurrent at similar power, gain, speed and noise parameters, while a Class AB topology is shown to handle a maximum photocurrent of 1.5mA.

1. INTRODUCTION

In conventional optical receivers, sufficient dynamic range can be achieved by placing an automatic gain control or limiting stage after the preamplifier. (e.g. [1]) However, the emergence of low-cost, user-driven optical applications such as wireless IR links, optical LAN technologies, and free space optics, require the receiver to handle a wider range of input signal levels. The combination of varying link lengths and large channel losses (due to propagation through legacy fiber or free space) mean that the dynamic range of the preamplifier must be enhanced. However, finding a balance between dynamic range and power consumption requirements can be a challenge, since keeping bias currents small degrades the preamplifier's ability to handle large signals.

Traditionally, preamplifiers with wide dynamic range have been achieved using variable gain transimpedance amplifiers (TIAs). A popular scheme (e.g. [2], [3]) uses MOS transistors biased in the triode region that vary their output resistances according to a control voltage obtained from a low-pass feedback loop. To eliminate the additional loop, limiting can be used to reduce gain. In [4] limiting is performed by diverting a portion of the input photocurrent, so that larger currents can be processed without affecting TIA performance under small photocurrents. However, even with limiting, dynamic range is limited when bias currents are small.

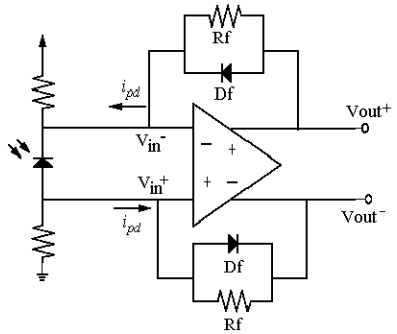


Fig. 1: Limiting TIA overview

This paper presents limiting techniques that improve the dynamic range of CMOS optical preamplifiers while minimizing power dissipation. The designs presented here are best suited for receivers operating below 100Mbps, where wide dynamic range, low power dissipation, and low cost are priorities. We compare three architectures using equations and simulation results. In section 2, we study the effects of limiting on a Cherry-Hooper TIA topology. In Section 3, we describe two dynamic biasing techniques that enable the TIA to handle photocurrents on the order of its bias currents, and in Section 4 we compare architectures and present simulation results.

2. BASIC LIMITING DESIGN

Fig. 1 shows a fully-differential TIA structure. Differential rather than single-ended photocurrent sensing is used to lower noise floor and improve sensitivity. Photodiode biasing details may be found in [5]. Fig. 2 details the topology of the limiting TIA. The design, based on [3], uses a two-stage Cherry-Hooper structure. Diode-connected NMOS transistors clamp the voltage across the fixed feedback resistors for large photocurrents.

For the half circuit in Fig. 2, the voltages at the inputs (V_{in}) and at the drains of $M_{1a,b}$ have a relatively small signal swing and are approximately equal if R_1 and R_f are the same. Thus diodes D_1 and D_f have the approximately the same voltage drop across them. These diodes shunt excess currents through the resistors so that the effective resistances seen by the TIA are approximately equal. Furthermore, the equality of R_1 and R_f

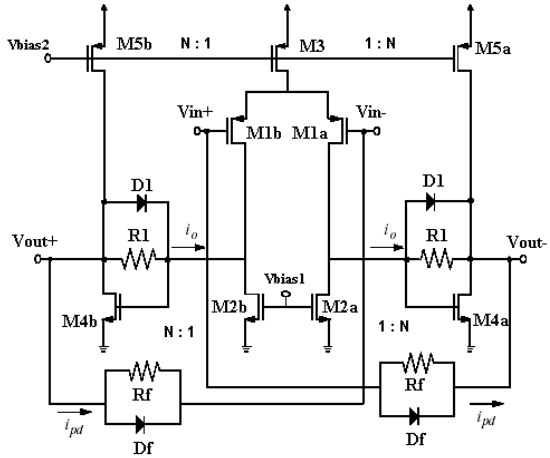


Fig. 2: Basic limiting TIA topology.

ensures that for moderate photocurrents, the internal current signal i_o will track photocurrent i_{pd} (currents as defined in Fig. 2).

The unity gain frequency of the TIA is given in (1). C_{PD} is the photodiode capacitance and g_{m1}, R_1, R_f are defined in Fig. 2.

$$\omega_t = \frac{g_{m1}R_1}{C_{PD}R_f} \tag{1}$$

As shown in [3], if R_1 tracks R_f, the unity gain frequency, ω_t, remains fixed in spite of changes to R_f so that stability is maintained. By extension, clamping R_1 and R_f equally ensures that the effective non-linear resistances track. Even when i_o reaches it maximum value so that it can no longer track i_{pd}, the effective resistances remain approximately the same so that stability is maintained.

Dynamic range for this TIA may be defined as the difference between the minimum detectable input level, equal to the input-referred noise floor, and the maximum photocurrent the amplifier can handle without excessive pulse distortion. To study the relationship between dynamic range and power dissipation, the upper bound on maximum photocurrent can be expressed relative to the total quiescent current in the amplifier, I_{TOT}. From Fig. 2, if I_{D4} and I_{D2} are the quiescent currents in $M_{4a,b}$ and $M_{2a,b}$ (per half circuit), and N is the ratio between these currents, then (2) characterizes power dissipation.

$$I_{TOT} = 2(I_{D4} + I_{D2}) = 2(1+N)I_{D2} \tag{2}$$

The drain current in $M_{4a,b}$ (per half circuit) is given in (3).

$$i_{D4} = I_{D4} \pm (i_{pd} + i_o) \tag{3}$$

From (3), when large photocurrents are present, the signal currents in M_{4b} will force it into the cutoff region, causing severe pulse width distortion. We therefore define $i_{pd}^{\max}$ as the upper bound on the photocurrent that can be absorbed by the TIA before M_{4b} goes into cutoff. Using (2)-(3) as shown in the appendix, an upper bound on dynamic range is given in (4).

$$i_{pd}^{\max} = \begin{cases} \dfrac{N}{4(N+1)} I_{TOT} & N < 2 \\ \dfrac{N-1}{2(N+1)} I_{TOT} & N > 2 \end{cases} \tag{4}$$

Using (2-4), I_{TOT} and N may be varied to optimize dynamic range and power dissipation.

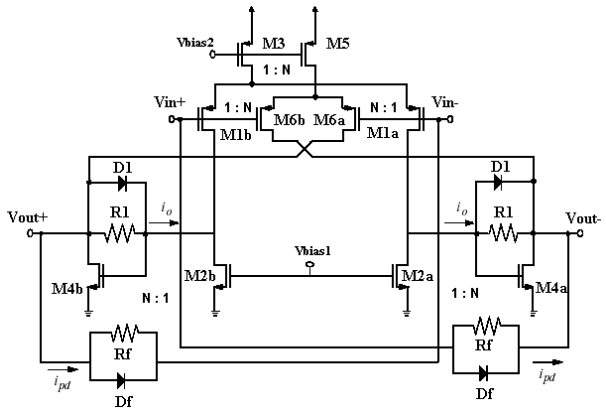


Fig. 3: Class A dynamic biasing topology.

3. DYNAMIC BIASING DESIGNS

In the design presented above, M_{4a} enters the triode region as it absorbs large currents, while M_{4b} enters the cutoff region as it loses drain current. Dynamic biasing can be used to increase the bias current in the half circuit where there is a shortage of current, while reducing the bias on the side where there is an excess. This technique achieves increased dynamic range with constant quiescent power dissipation, and has been used in a variety of applications (see for example [6]). We propose two dynamic biasing schemes that complement the limiting TIA design presented above.

3.1. Class A Dynamic Biasing

The first dynamic biasing topology, similar to [7], uses the input nodes of the amplifier to detect large signal currents. We designate this topology as Class A because the total bias current in the TIA remains constant. As shown in Fig. 3, the drain current of $M_{6a,b}$ mirrors the current through $M_{1a.b}$. Because the drain of $M_{6a,b}$ is cross-coupled to the output node, it pushes a signal current through $M_{4b,a}$ that is proportional and opposite to internal current i_o. If N the ratio between $M_{6a,b}$ and $M_{1a,b}$, then (5) characterizes power dissipation in the TIA, while (6) describes the drain current in $M_{4a,b}$. Following an analysis as in the appendix, (7) gives an upper bound on dynamic range.

$$I_{TOT} = 2(I_{D1} + I_{D6}) = 2(1+N)I_{D1} \tag{5}$$

$$i_{D4} = I_{D4} \pm (i_{pd} + i_o - N \cdot i_o) \tag{6}$$

$$i_{pd}^{\max} = \begin{cases} \dfrac{1}{2-N} \dfrac{N}{2(N+1)} I_{TOT} & N < 1 \\ \dfrac{2N-1}{2(N+1)} I_{TOT} & N > 1 \end{cases} \tag{7}$$

3.2. Class AB Dynamic Biasing

The second dynamic biasing scheme, similar to [8], is shown in Fig. 4. We designate this topology as Class AB because the total bias current in the TIA increases under large photocurrents. A transconductor (transistors $M_{6,-9}$) varies the bias currents in $M_{4a,b}$. The current through $M_{4a,b}$ is mirrored by $M_{6a,b}$ according

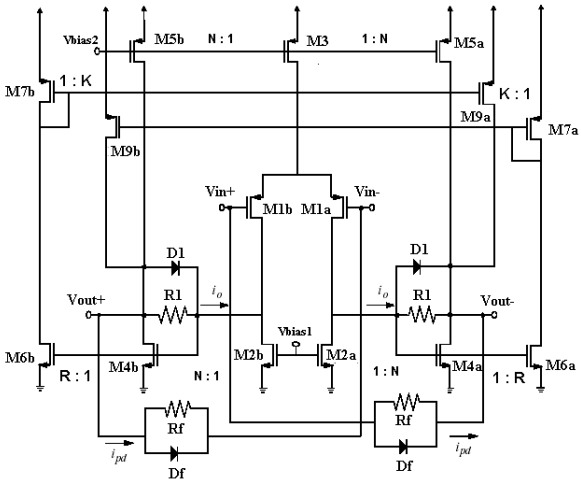


Fig. 4: Class AB dynamic biasing topology.

to ratio R. The current through $M_{6a,b}$ sets the current through $M_{7a,b}$. $M_{7a,b}$ then sets the currents sourced into $M_{4b,a}$ by $M_{9b,a}$ according to ratio K.

Assuming ideal mirroring, the drain currents in $M_{4a,b}$ can be found from KCL at the output nodes.

$$\begin{cases} i_{D4a} = I_{D5} + KRi_{D4b} + i_{pd} + i_o \\ i_{D4b} = I_{D5} + KRi_{D4a} - i_{pd} - i_o \end{cases} \quad (8)$$

Solving (8) under quiescent conditions yields (9), leading to the condition $I_{D5} \neq 0$ and $RK < 1$ for stable biasing.

$$I_{D4} = \frac{I_{D5}}{1 - RK} \quad (9)$$

When a photocurrent is injected into the preamplifier, the drain current of M_{4b} decreases while the drain current of M_{4a} increases. Because the gates of $M_{9a,b}$ are cross-coupled to $M_{7a,b}$, the drain current of M_{9b} will increase to balance the loss of current through M_{4b}, while the opposite occours for M_{9a} and M_{4a}. This can be seen from (10), which combines (8)-(9) to gives current flow in $M_{4a,b}$ (per half circuit).

$$i_{D4} = I_{D4} \pm \frac{i_{pd} + i_o}{1 + RK} \quad (10)$$

Following the analysis used for previous designs, (11) characterizes quiescent power dissipation, and (12) gives an upper bound on the dynamic range.

$$I_{TOT} = 2(I_{D2} + I_{D4} + I_{D6}) = 2(1 + N + NR) \cdot I_{D2} \quad (11)$$

$$i_{pd}^{\max} = \begin{cases} \dfrac{(1+KR)\cdot N}{4(1+N+NR)} I_{TOT} & N < \dfrac{2}{1+KR} \\ \dfrac{(1+KR)\cdot N - 1}{2(1+N+NR)} I_{TOT} & N > \dfrac{2}{1+KR} \end{cases} \quad (12)$$

When designing the circuit, we set $R<1$ so that minimal power is dissipated by the transconductor. To magnify the effects of dynamic biasing we take K large while ensuring $RK<1$. Finally, we may vary N and I_{TOT} to optimize dynamic range and power dissipation.

From Fig. 5, a sweep of i_{D4b} versus increasing photocurrent, we can determine the simulated upper bound on the photocurrent ($i_{pd}^{\max}$) by finding the photocurrent that forces M_{4b} into cutoff (i.e. $i_{D4b} = 0$). From Fig. 5 we can also observe that the upper limit on dynamic range can extend well beyond the limit in (12). For small photocurrents, the currents in $M_{4a,b}$ are as in (10). However, when i_{pd} increases, the ideal current mirroring assumption becomes invalid. Large photocurrents force M_{4a} into the triode region while M_{6a} remains in the active region. Thus, M_{6a} will overestimate the amount of current flowing through M_{4a}, so that the transconductor sources more current into M_{4b} than predicted by (10). Eventually, the drain current in M_{4b} (i_{D4b}) will begin to *increase* with increasing photocurrent. Furthermore, since i_{D4b} sets i_{D4a}, i_{D4a} will also increase above the value predicted by (10). Finally, the large currents in M_{6a} will force it into the triode region, limiting that amount of current the transconductor can supply so that i_{D4b} once again decreases with increasing photocurrent. Thus all bias currents in the circuit increase for the duration of the large photocurrent pulse, improving dynamic range at the cost of increased *dynamic* power dissipation.

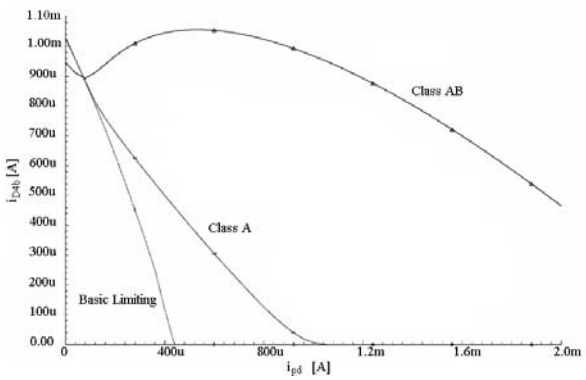


Fig. 5: Simulated sweep of i_{D4b} versus i_{pd}. All designs have I_{ToT} about 3mA and N=2.5. Class AB has (R,K)=(1/9,7).

4. RESULTS AND DISCUSSION

Fig. 6 is a plot of the calculated upper bound on dynamic range assuming ideal current mirroring ($i_{pd}^{\max}$) for various values of N as given by (4), (7), and (12). We can see that for constant quiescent power (i.e constant I_{TOT}), dynamic biasing raises the upper bound on the dynamic range. Setting N=2.5 for example, gives $i_{pd}^{\max} / I_{TOT} \cong 20\%$ for the basic limiting design, which improves to about 60% and 45% for the Class A and Class AB design respectively (Class AB has (R,K) = (1/9,7)).

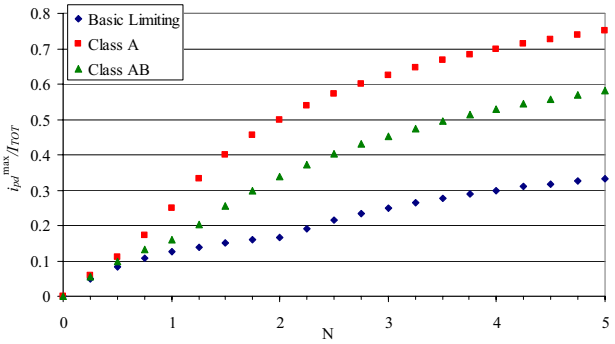


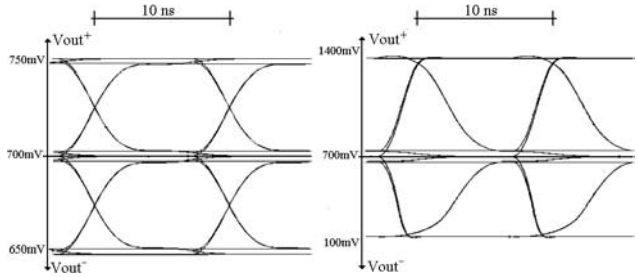
Fig. 6: Calculated upper bound on dynamic range ($i_{pd}^{\max}$) normalized over I_{TOT} and plotted versus N. Class AB has (R,K) = (1/9,7)

All three designs were simulated in a 0.35um CMOS technology with V_{DD}=3.3V and a transimpedance gain of 5kΩ. From Fig. 5, we note that imperfect mirroring causes the simulated upper bound on photocurrent for the Class AB topology to significantly exceed the calculated upper bound (see section 3.2). In fact, contrary to the predictions made by (7) and (12), imperfect mirroring causes simulated upper bound on the Class AB architecture to surpass that of Class A architecture.

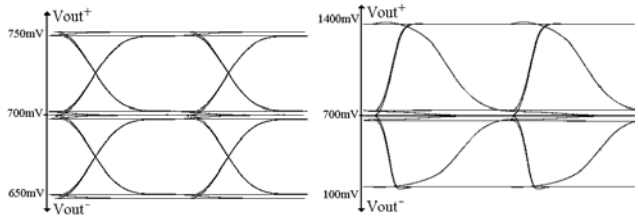
Each design was tested with a C_{PD}=5pF, typical of an IR wireless photodiode [3]. Fig. 6 shows positive and negative output eye diagrams for small and maximum photocurrents at 100Mbps, while Table 1 provides relevant parameters for the three topologies. Eye diagrams were used to determine the maximum photocurrent handled by the TIA without excessive pulse distortion.

	Basic	Class A	Class AB
Ratios	N=2.5	N=2.5	N=2.5 R=1/9 K=7
I_{TOT}	2.83 mA	2.84 mA	2.91 mA
Maximum i_{pd}	400 uA	800 uA	1.5 mA
i_{RMS}	177 nA	167 nA	184 nA
Dynamic Range	67 dB	74 dB	79 dB
Bandwidth	83 MHz	81 MHz	85 MHz

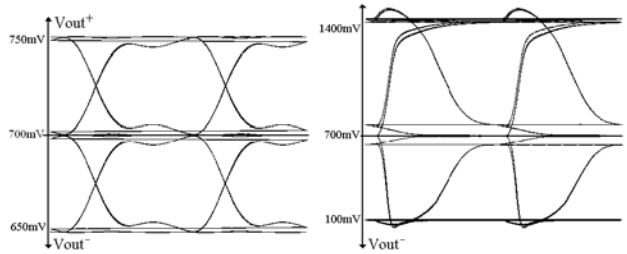
Table 1: Summary of parameters from simulations. (i_{RMS} integrated between 100kHz to 166MHz.)



a) Basic limiting design, i_{pd} = 10uA, 400uA.



b) Class A dynamic biasing, i_{pd} =10uA, 800uA.



c) Class AB dynamic biasing, i_{pd} =10uA, 1.5mA.

Fig. 7: Simulated positive and negative output eye-diagrams for small and maximum photocurrents at 100Mbps.

The left half of Fig. 7 shows the undistorted eye diagrams for small i_{pd} while the right half shows eye diagrams at the specified maximum i_{pd}. For all three designs, pulse width distortion is observed at maximum photocurrent levels due to the clamping behavior of the limiting preamplifers. Because the clamping threshold is set to a fraction of the maximum i_{pd}, strong optical pulses are widened, while gaps between the optical pulses are shortened. The resulting eye diagram is asymmetrical with crossover points near the outer edges of the eye. Symmetry may be reestablished by removing the intrinsic dc offset in i_{pd} and replacing each individual diode in Figs.1-4 with two parallel, opposite-facing diodes. In this way, the rising and falling edges may be clamped at the same point in the eye, causing the crossover points to occur in the middle of the eye.

7. CONCLUSIONS

We have presented new methods of increasing dynamic range while minimizing power consumption of optical preamplifiers operating below 100Mbps. A fully-differential Cherry-Hooper topology using diode clamping to limit gain has been designed and simulated. To improve dynamic range, we have introduced dynamic biasing to compensate for excesses or shortages in drain currents. Simulations have shown that a Class A dynamic biasing topology doubled dynamic range without increasing power dissipation. A Class AB dynamic biasing topology has been simulated to handle almost four times the photocurrent handled by the basic limiting design.

8. REFERENCES

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9. APPENDIX

The following outlines the method used to determine the upper limit on the dynamic range of the limiting TIA in Fig. 2.

Because i_o is supplied by M_3, $i_o \le \frac{1}{2} I_{D3} = I_{D2}$. We assume that the equality of R_f and R_1 ensures that i_o tracks i_{pd} whenever $i_{pd} \le I_{D2}$. Thus when M_{4b} is forced into cutoff by $i_{pd}^{\max} \le I_{D2}$, setting $i_{D4}=0$ in (2), we arrive at the condition in (13).

$$i_{pd}^{\max} = \frac{I_{D4}}{2} \quad \text{when} \quad i_{pd}^{\max} \le I_{D2} \tag{13}$$

Using (3) to express I_{D4}, I_{D2} in terms of I_{TOT}, we rewrite (13) as (14).

$$i_{pd}^{\max} = \frac{N \cdot I_{TOT}}{4(N+1)} \quad \text{when} \quad \frac{N \cdot I_{TOT}}{4(N+1)} \le \frac{I_{TOT}}{2(N+1)} \tag{14}$$

Solving the inequality we find (14) holds whenever $N \le 2$.

When M_{4b} is forced into cutoff by $i_{pd}^{\max} \ge I_{D2}$, setting $i_{D4}=0$ in (2), and noting that i_o no longer tracks i_{pd} we find (15).

$$i_{pd}^{\max} = I_{D4} - I_{D2} \quad \text{when} \quad i_{pd}^{\max} \ge I_{D2} \tag{15}$$

Using (3) and solving the inequality as before gives (16).

$$i_{pd}^{\max} = \frac{(N-1) I_{TOT}}{2(N+1)} \quad \text{when} \quad N \ge 2 \tag{16}$$

The combination of (14) and (16) gives (4).